DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set

forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this

application is eligible for continued examination under 37 CFR 1.114, and the fee set

forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action

has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on

9/16/2011 has been entered.

Response to Amendment

2.   **Claims 1, 14-15, 22, 31, 45 and 49** have been amended.

3.   **Claims 1-47, and 49-54** are pending.

Response to Arguments

4.   Regarding prior art rejection, applicant's arguments with respect to **claims 1-47,**

and 49-54 have been considered, but they are moot because of the new ground of

rejections.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6.   **Claims 1-11, 14-23, 27, 31-41, 43-45, 49, 51, and 53-54** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto (US 5,646,688) in view of Ryan (US 6,263,019), and further in view of Akihiro (JP 2003-152546) hereafter referenced as Hashimoto and Ryan and Akihiro, respectively.

Regarding **claim 1**, Hashimoto discloses Video Decoder Architecture Using Separate Semiconductor Substrates. Specifically Hashimoto discloses A video decoding circuit (video data decoding system, Fig.1) comprising:
a first video data processor (first semiconductor substrate 12, Fig.1) ; a second video data processor (second semiconductor substrate 14, Fig.1); and a connection connecting (buses internal, col.2, line 40) said first video data processor and said second data processor; wherein said first video data processor is arranged to receive a first signal comprising encoded video data (encoded input, col.2, line 44), process said first signal to provide a second signal and output said second signal (motion vector and IDCT output, Fig.1), said first video data processor being arranged to process said first signal dependent on at least part (decoding motion vectors by parser 20 and dequantizing the quantized DCT coefficients by 22 and 24, Fig.1) of said received first signal, and said second video data processor comprising a predictor constructor (Motion compensation unit 26a, Fig.1), said second video data processor is arranged to receive at least a part of said second signal (motion vector and IDCT output, Fig.1), process said at least a part of said second signal (motion vector and IDCT output, Fig.1) to provide a third signal (I-picture, B-picture, and P-picture, Fig.1), and output said third

signal (output, fig.1), said second and third signals comprising a decoded video image

stream (motion vector, IDCT output, I-picture, B-picture, and P-picture, Fig.1); and

said second video data processor is arranged to process said at least part of said

second signal (motion vector and IDCT output, Fig.1) dependent on the format of the

data received. However, Hashimoto is silent on wherein a part of said second signal

comprises a picture level parameter word which comprises coding standard information,

said coding standard information indicating which of a plurality of encoding methods

was used to encode the encoded video data.

In the analogous field of endeavor, Akihiro discloses Multi-Format Stream

Decoder and Multi-Format Stream Sender. Specifically Akihiro discloses embedding

coding standard information (mean for adding format identifier 42, Fig.4) indicating

which of a plurality of encoding methods was used to encode the encoded video data in

front of the bitstream (0x01 for Real Video, 0x02 for MPEG video, 0x03 for MPEG4,

par.60), in order for the decoder to select the decoder accordingly (extracting format

identifier 52, selecting decoder 53, Fig.5).

Therefore, given this teaching, it would have been obvious to one of ordinary skill

in the art at the time invention was made to modify Hashimoto by specifically providing

embedding coding standard information (mean for adding format identifier 42, Fig.4)

indicating which of a plurality of encoding methods was used to encode the encoded

video data in front of the bitstream, in order for the decoder to select the decoder

accordingly. However, Hashimoto and Akihiro still fail to disclose wherein a part of said

second signal comprises a picture level parameter word a picture level parameter word
comprising said coding standard information data.

In the analogous field of endeavor, Ryan discloses Variable Rate MPEG-2 Video
Syntax Processor. Specifically Ryan discloses wherein a part of said second signal
comprises a picture level parameter word (picture layer of syntax are parsed by
Microprocessor, col.5 , line 46-48; Picture Decode parameters 218, Fig.2), in order to
provide information to decode slice and macroblock record in the MPEG standard video
bitstream (col.5, line 49-52).

Therefore, it was obvious to embed the coding standard information data into the
picture level header as well as into the front of the bitstream, in order to secure the
transmission of the format identifier in the case of the transmission error. The
Hashimoto video data processing architecture, incorporating the Akihiro embedding
coding standard information in front of the bitstream, further incorporating embedding
the coding standard information into the Ryan picture level header, has all the features
of claim 1.

Regarding **Claim 2**, Hashimoto and Ryan and Akihiro disclose everything
claimed as applied above (see claim 1). In addition, Hashimoto discloses wherein said
first video data processor is arranged to variable length decode (decode Huffman-
encoding, col.3, line 15-16) said received first signal to produce a decoded first signal.

Regarding **Claim 3**, Hashimoto and Ryan and Akihiro disclose everything
claimed as applied above (see claim 2). In addition, Hashimoto discloses wherein said
first video data processor is arranged to separate said first signal data into at least a first

part and a second part, wherein said first part comprises at least one of:

pixel data (Input to Dequantization (22, Fig.1) when macroblock is intra type);

residual data (Input to Dequantization (22, Fig.1) when macroblock is inter type), and

wherein said second part comprises motion vector data (motion vector, Fig.1).

Regarding **Claim 4**, Hashimoto and Ryan and Akihiro disclose everything

claimed as applied above (see claim 3). In addition, Hashimoto discloses wherein said

first video data processor is arranged to inverse quantize (Dequantization 22, Fig.1)

said first part of said first signal.

Regarding **Claim 5**, Hashimoto and Ryan and Akihiro disclose everything

claimed as applied above (see claim 3). In addition, Hashimoto discloses wherein said

first video data processor is arranged to spatial domain transform (IDCT 24, Fig.1) said

first part of said first signal.

Regarding **Claim 6**, Hashimoto and Ryan and Akihiro disclose everything

claimed as applied above (see claim 4). In addition, Hashimoto discloses wherein said

first video data processor (first semiconductor substrate 12, Fig.1) is arranged to

combine (examiner read it as combining two data output to feed them to the second

semiconductor substrate as shown in Fig.1) said inverse quantized (output of

Dequantization 22, Fig.1) first part (Input to Dequantization (22, Fig.1) of said first signal

with said second part (Motion Vector, Fig.1) of said first signal.

Regarding **Claim 7**, Hashimoto and Ryan and Akihiro disclose everything

claimed as applied above (see claim 1). In addition, Hashimoto discloses wherein said

second video data

processor is arranged (calculate motion compensated frame, col.4, line 38-40) to

interpolate (averaging values for neighboring pixels, col.4, line 45-46) at least a first part

(output of IDCT 24,Fig.1, which is image pixel data) of said second signal..

Regarding **Claim 8**, Hashimoto and Ryan and Akihiro disclose everything

claimed as applied above (see claim 7). In addition, Hashimoto discloses wherein said

second video data

processor is arranged (calculate motion compensated frame, col.4, line 38-40) to

interpolate at least a first part (IDCT(24,Fig.1) output, which is an image pixel data) of

said second signal using one of horizontal and vertical interpolation (averaging values

for neighboring pixels, col.4, line 45-46).

Regarding **Claim 9**, Hashimoto and Ryan and Akihiro disclose everything

claimed as applied above (see claim 8). In addition, Hashimoto discloses further

comprising a memory (input buffer 30 and 36, Fig.1), said second video data processor

being arranged to store said interpolated part of said second signal in said memory.

Regarding **Claim 10**, Hashimoto and Ryan and Akihiro disclose everything

claimed as applied above (see claim 8). In addition, Hashimoto discloses wherein said

second video data processor is arranged to interpolate said stored interpolated first part

of said second signal using the other one of horizontal and vertical interpolation (it was

well known in the art that when half pixel position is at the center of four surrounding

pixels, it is interpolated in one direction (horizontally or vertically) first (horizontally for

top and bottom, or vertically for left and right of half pixel position) and then interpolate

(average) in the other direction).

Regarding **Claim 11**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 7). In addition, Hashimoto discloses wherein said second video data processor is arranged to combine (summation unit (42, fig.1) sum, col.4, line 39-43) said interpolated part (compensated frame, col.4, line 39-43) of said second signal and a further part (differential signal (IDCT output, Fig.1), col.4, line 39-43) of said second signal, wherein said interpolated part of said second signal comprises an estimated macro block (prediction, col.1, line 40-42), and said further part of said second signal comprises residual error data (differential data, col.1, line 40-42).

Regarding **Claim 14**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 1). In addition, Akihiro discloses wherein said coding standard information defines variations in the type of data (0x01 for Real Video, 0x02 for MPEG video, 0x03 for MPEG4, par.60).

Regarding **Claim 15**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 14). In addition, Hashimoto discloses wherein said connection comprises a bus (buses internal, col.2, line 40) connecting said first and second video data processors, and wherein the circuit further comprising a memory device (Input Buffer 28, Fig.1), said memory device being connected to said bus (buses internal, col.2, line 40).

Regarding **Claim 16**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 15). In addition, Hashimoto discloses wherein said first video data processor has an output (IDCT (24, Fig.1) output) for outputting said second signal to said memory device (Input Buffer 28, Fig.1) via said bus.

Regarding **Claim 17**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 16). In addition, Hashimoto discloses wherein said second video data processor has an input (input to Input buffer 28, fig.1) for receiving said parts of said second signal from said memory device via said bus.

Regarding **Claim 18**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 1). In addition, Hashimoto discloses wherein said connection comprises a data interconnect (8-bit buses, col.5, line 54-58) said data interconnect directly (As shown in Fig.1, the buses are dedicated between two processors, therefore they are interconnect directly) connecting said first video data processor and said second video data processor.

Regarding **Claim 19**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 18). In addition, Hashimoto discloses wherein said first video data processor has an output for outputting said second signal (8-bit bus for motion vectors and 8-bit bus to provide for input to input buffer 28, col.5, line 54-58) to said data interconnect.

Regarding **Claim 20**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 18). In addition, Hashimoto discloses wherein said second video data processor has an input (input to input buffer 28) for receiving said parts of said second signal from said data interconnect.

Regarding **Claim 21**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 20). In addition, Hashimoto discloses wherein said connection comprises a bus (8-bit bus for motion vectors and 8-bit bus to provide for

input to input buffer 28, col.5, line 54-58) connecting said first and second video data

processors and further comprising a memory device (input to input buffer 28, col.5, line

54-58), said memory device being connected to said bus wherein said second video

data processor receives part of said parts of said second signal from said data

interconnect (bus is also data interconnect) and part of said parts of said second signal

from said bus.

Regarding **Claim 22**, the Hashimoto video data processing architecture,

incorporating the Akihiro embedding coding standard information in front of the

bitstream, further incorporating embedding the coding standard information into the

Ryan picture level header, as applied to the claim 1, teaches wherein the coding

standard information indicates a format of the encoded video data representing to the

encoding method used to encode the encoded video data (Akihiro: 0x01 for Real Video,

0x02 for MPEG video, 0x03 for MPEG4, par.60), and wherein said first signal is at least

one of a MPEG2 encoded video stream (Hashimoto: MPEG, col.4, line 6); a H. 263

encoded video stream; a RealVideo9 encoded video stream; a Windows media player

encoded video stream; a H. 264 encoded video stream.

Regarding **Claim 27**, Hashimoto and Ryan and Akihiro disclose everything

claimed as applied above (see claim 1). In addition, Hashimoto discloses An integrated

circuit (first and second semiconductor substrates 12 and 14, Fig.1) comprising a circuit.

Regarding **Claim 31**, the claim is a method claim corresponding to the apparatus

claim 1. Therefore, it is rejected for the same reason as claim 1.

Regarding **Claim 32**, the claim is a method claim corresponding to the apparatus claim 2. Therefore, it is rejected for the same reason as claim 2.

Regarding **Claim 33**, the claim is a method claim corresponding to the apparatus claim 3. Therefore, it is rejected for the same reason as claim 3.

Regarding **Claim 34**, the claim is a method claim corresponding to the apparatus claim 4. Therefore, it is rejected for the same reason as claim 4.

Regarding **Claim 35**, the claim is a method claim corresponding to the apparatus claim 5. Therefore, it is rejected for the same reason as claim 5.

Regarding **Claim 36**, the claim is a method claim corresponding to the apparatus claim 6. Therefore, it is rejected for the same reason as claim 6.

Regarding **Claim 37**, the claim is a method claim corresponding to the apparatus claim 7. Therefore, it is rejected for the same reason as claim 7.

Regarding **Claim 38**, the claim is a method claim corresponding to the apparatus claim 8. Therefore, it is rejected for the same reason as claim 8.

Regarding **Claim 39**, the claim is a method claim corresponding to the apparatus claim 9. Therefore, it is rejected for the same reason as claim 9.

Regarding **Claim 40**, the claim is a method claim corresponding to the apparatus claim 10. Therefore, it is rejected for the same reason as claim 10.

Regarding **Claim 41**, the claim is a method claim corresponding to the apparatus claim 11. Therefore, it is rejected for the same reason as claim 11.

Regarding **Claim 43**, the claim is a method claim corresponding to the apparatus claim 16. Therefore, it is rejected for the same reason as claim 16.

Regarding **Claim 44**, the claim is a method claim corresponding to the apparatus claim 18. Therefore, it is rejected for the same reason as claim 18.

Regarding **Claim 45**, the claim is a method claim corresponding to the apparatus claim 21. Therefore, it is rejected for the same reason as claim 21.

Regarding **Claim 49**, the claim is a computer readable storage device claim corresponding to the apparatus claim 1. Therefore, it is rejected for the same reason as claim 1.

Regarding **Claim 51**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 1). In addition, Hashimoto discloses An MPEG decoder (decoding a MPEG data stream, col.4, line 4-6) comprising a circuit as claimed in claim 1.

Regarding **Claim 53**, Hashimoto and Ryan and Akihiro disclose everything claimed as applied above (see claim 5). In addition, Hashimoto discloses wherein said first video data processor (first semiconductor substrate 12, Fig.1) is arranged to combine said spatial domain transformed (output of IDCT 24, Fig.1) first part (Input to Dequantization (22, Fig.1) of said first signal with said second part (Motion Vector, Fig.1) of said first signal.

Regarding **Claim 54**, the claim is a method claim corresponding to the apparatus claim 53. Therefore, it is rejected for the same reason as claim 53.

7. **Claims 12-13, and 42** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hashimoto, in view of Ryan, further in view of Akihiro, and further in view of Gomila (US 2003/0,206,664) (hereafter referenced as Gomila).

Regarding **claim 12**, Hashimoto and Ryan and Akihiro disclose everything

clamed as applied above (see claim 11). However Hashimoto and Ryan and Akihiro fail

to disclose wherein said second video data processor is arranged to filter at least one of

said at least one part of said second signal and said third signal.

In the analogous field of endeavor, Gomila discloses Deblocking Filter

Conditioned on Pixel Brightness. Specifically Gomila discloses deblocking *filtering* of

reconstructed signal (*said third signal)* (Deblocking Filter 240, Fig.2), in order to reduce

blockiness artifact (paragraph 4).

Therefore, given this teaching, it would have been obvious to one of ordinary skill

in the art at the time invention was made to modify Hashimoto and Ryan ad Akihiro by

specially incorporating deblocking filter in the second video data processor, in order to

reduce blockiness artifact. The Hashimoto video data processing architecture,

incorporating the Akihiro embedding coding standard information in front of the

bitstream, further incorporating embedding the coding standard information into the

Ryan picture level header, further incorporating the Gomila deblocking filter in the

second semiconductor substrate, has all the features of claim 12.

Regarding **claim 13**, the Hashimoto video data processing architecture,

incorporating the Akihiro embedding coding standard information in front of the

bitstream, further incorporating embedding the coding standard information into the

Ryan picture level header, further incorporating the Gomila deblocking filter in the

second semiconductor substrate, as applied to claim 12, discloses wherein said filter

comprises at least one of a de-ringing filter and a deblocking filter *)* (Gomila: Deblocking

Filter 240, Fig.2).

Regarding **Claim 42**, the claim is a method claim corresponding to the apparatus

claim 13. Therefore, it is rejected for the same reason as claim 13.

8.   **Claim 23, 30, 50, and 52** are rejected under 35 U.S.C. 103(a) as being

unpatentable over Hashimoto in view of Ryan, further in view of Akihiro, and further in

view of official notice.

Regarding **Claim 23**, Hashimoto and Ryan and Akihiro disclose everything

claimed as applied above (see claim 1). In addition, Hashimoto discloses wherein said

second signal comprises at least one of: buffer base address word; picture level

parameter header word; macro-block header word; slice parameter word; motion vector

horizontal luma word (motion vector, Fig.1, and it was well known that motion vector

consist of a luma horizontal and vertical components); motion vector vertical luma word

(motion vector, Fig.1, and it was well known that motion vector consist of a luma

horizontal and vertical components); motion vector horizontal chroma word ; motion

vector vertical chroma word; pixel data reference word and pixel data residual word

(IDCT output, Fig.1).

Regarding **claim 30**, Hashimoto and Ryan and Akihiro disclose everything

clamed as applied above (see claim 1). However Hashimoto fails to disclose wherein

said second video data processor comprises a programmable processor.

However, it was well known in the art that the functions of second video

processor is performed by programmable processor such as DSP (digital signal

processor), in order to have a flexibility of programming.

Therefore, given this teaching, it would have been obvious to one of ordinary skill

in the art at the time invention was made to modify Hashimoto by specially providing

DSP to the second video processor, in order to have a flexibility of programming. The

Hashimoto video data processing architecture, incorporating DSP to the second video

processor, has all the features of claim 30.

Regarding **claim 50**, Hashimoto and Ryan and Akihiro disclose everything

clamed as applied above (see claim 1). However Hashimoto fails to disclose A Digital

Versatile Disc device comprising a circuit as claimed in claim 1.

However, it was well known in the art that DVD is storing MPEG encoded

bitstream. Therefore, it requires MPEG decoder and the Hashimoto MPEG video

decoder architecture is obvious to try to use, in order to play DVD movie.

Regarding **claim 52**, Hashimoto and Ryan and Akihiro disclose everything

clamed as applied above (see claim 1). However Hashimoto fails to disclose A Digital

Video Broadcasting device comprising a circuit as claimed in claim 1.

However, it was well known in the art that DVB broadcasting is using MPEG

standard bitstream. Therefore, DVB receiver requires MPEG decoder and the

Hashimoto MPEG video decoder architecture is obvious to try to use, in order to play

the video transmitted by DVB broadcasting.

9.   **Claims 24-26, and 46-47** are rejected under 35 U.S.C. 103(a) as being

unpatentable over Hashimoto in view of Ryan, further in view of Akihiro, and further in

view of Wu (US 6,415,345) (hereafter referenced as Wu).

Regarding **claim 24**, Hashimoto and Ryan and Akihiro disclose everything

clamed as applied above (see claim 11). However Hashimoto and Ryan and Akihiro fail

to disclose wherein said first video data processor comprises a data packer.

In the analogous field of endeavor, Wu discloses Bus Mastering Interface Control

System for Transferring Multistream Data over a Host Bus. Specifically Wu discloses

data packer (122 at Fig.1) with a host bus (108, Fig.1), in order to pack valid data in

fixed sized unit to form a packet (col.3, line 47-50).

Therefore, given this teaching, it would have been obvious to one of ordinary skill

in the art at the time invention was made to modify Hashimoto and Ryan and Akihiro by

specifically incorporating data packer in the first video data processor with a host bus

between first and second video data processors, in order to pack valid data in fixed

sized unit to form a packet. The Hashimoto video data processing architecture,

incorporating the Akihiro embedding coding standard information in front of the

bitstream, further incorporating embedding the coding standard information into the

Ryan picture level header, further incorporating the Wu data packer in the first video

data processor with a host bus, has all the features of claim 24.

Regarding **claim 25**, the claimed invention is same as claim 24 except that data

packer is in the second video processor instead of first. Two claimed inventions are

equivalent and one is an obvious variation of the other. And therefore, it is obvious over

Hashimoto in view of Wu.

Regarding **claim 26**, the Hashimoto video data processing architecture,

incorporating the Akihiro embedding coding standard information in front of the

bitstream, further incorporating embedding the coding standard information into the

Ryan picture level header, further incorporating the Wu data packer in the first video

data processor with a host bus, as applied to claim 24, discloses wherein said data

packer comprises: an input (Wu: input to bus mater FIFO controller 124, Fig.1), said

input being arranged to receive said second signal (Hashimoto: motion vector and IDCT

output, Fig.1), said second signal comprising data words (Hashimoto: motion vectors

and IDCT output); means for ordering said data words (Wu: pack valid data in fixed

sized unit to form a packet, col.3, line 47-50);

and an output (Wu: output to host bus 108, Fig.1), said output being arranged to

transmit data packets comprising ordered data words.

Regarding **Claim 46**, the claim is a method claim corresponding to the apparatus

claim 24. Therefore, it is rejected for the same reason as claim 24.

Regarding **Claim 47**, the claim is a method claim corresponding to the apparatus

claim 26. Therefore, it is rejected for the same reason as claim 26.

10.   **Claims 28-29** are rejected under 35 U.S.C. 103(a) as being unpatentable over

Hashimoto in view of Ryan, further in view of Akihiro, and further in view of Trivedi (US

6,573,846) (hereafter referenced as Trivedi).

Regarding **claim 28**, Hashimoto and Ryan and Akihiro disclose everything

clamed as applied above (see claim 1). However Hashimoto and Ryan and Akihiro fail

to disclose wherein said first video data processor comprises a very long instruction

word processor.

In the analogous field of endeavor, Trivedi discloses Method and Apparatus for

Variable Length Decoding and Encoding of Video Stream. Specifically Wu discloses

wherein said first video data processor comprises a very long instruction word

processor (Media Processor using very long instruction word (VLIW), Fig.5A) for

decoding MPEG bitstream such VLD (Variable length decoding) (8303, Fig.63) and

IDCT (8304 at Fig.63), in order to issue the instructions to different functional units in

the media processor in the same clock cycle (col.2, line 17-24).

Therefore, given this teaching, it would have been obvious to one of ordinary skill

in the art at the time invention was made to modify Hashimoto and Ryan and Akihiro by

specifically providing VLIW processing to the first video processor, in order to issue the

instructions to different functional units in the media processor in the same clock cycle.

the Hashimoto video data processing architecture, incorporating the Akihiro embedding

coding standard information in front of the bitstream, further incorporating embedding

the coding standard information into the Ryan picture level header, further incorporating

the Trivedi VLIW processing architecture to the first video processor, has all the

features of claim 28.

Regarding **claim 29**, the Hashimoto video data processing architecture,

incorporating the Akihiro embedding coding standard information in front of the

bitstream, further incorporating embedding the coding standard information into the

Ryan picture level header, further incorporating the Trivedi VLIW processing

architecture to the first video processor, as applied to claim 28, discloses wherein said

very long instruction word processor is adapted to process said first signal further

(Trivedi: conventional media processor may use very long instruction word

programming, col.2, line 17-18) dependent on a set of instructions stored in a memory

(Trivedi: cache 1504 and host memory 1506, Fig.5A) .

Conclusion

11.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to HEE-YONG KIM whose telephone number is (571)270-

3669. The examiner can normally be reached on Monday-Thursday, 8:00am-5pm EST.

   If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Christopher Kelley can be reached on 571-272-7331. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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